Product Preview 155Mb/s / 622Mb/s Transmitter (Multiplexer) with Clock Generation

The MC10SX1405 transmitter (Tx) chip is an integrated serialization SONET OC-3 (155.52Mb/s) and OC-12 (622.08 Mb/s) interface device. It generates the line rate clock and performs parallel-to-serial conversion in conformance with SONET/SDH transmission standards. High performance and low power is achieved with MOSAIC VTM, Motorola's most advanced high-performance silicon Bipolar process. A companion de-serialization (Rx) chip, the SX1401, is also available.

- Selectable eight or four bit parallel interface
- Performs parallel-to-serial conversion of four 38.88 Mbit/s or eight 19.44 Mbit/s inputs to a 155.52 Mbit/s OC3 serial data output
- Performs parallel-to-serial conversion of eight 77.76 Mbit/s inputs to a 622.08 Mbit/s OC12 serial data output
- Integrated PLL and VCO to generate the line-rate clock from a sub-rate reference clock
- Multiple configurations for parallel interface timing provide system design versatility
- Provides PLL Frequency Control Monitor and Out-of-Lock Indicator
- Provides parity verification of the OC3/OC12 serial output stream
- Single supply operation (+5V)

APPLICATIONS

- SONET/SDH-based transmission systems, modules, test equipment
- ATM using SONET
- Add drop multiplexers
- Other (non-SONET) data rate transmission systems

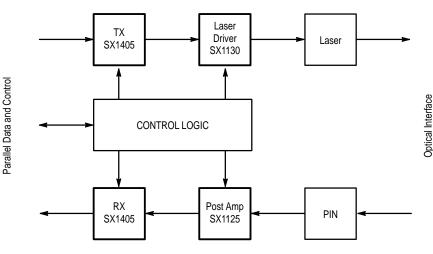


Figure 1. Typical OC3/OC12 Electro–Optical Interface

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC10SX1405

TRANSMITTER (MULTIPLEXER) WITH CLOCK GENERATION





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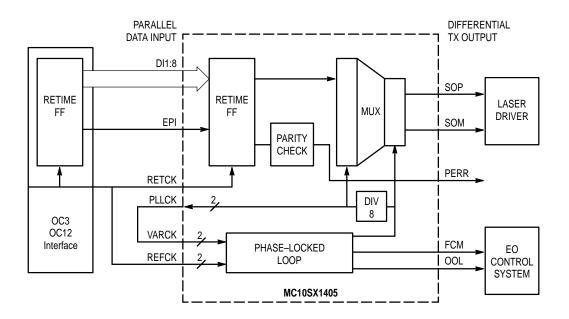


Figure 2. MC10SX1405 Simplified Block Diagram

SX1405 Theory of Operation

Operation of the SX1405 is straightforward. Parallel data is input to the device. Serial-to-parallel conversion is performed. Then the serial data is output at the selected line rate clock. The 78 MByte/s or 19 MByte/s parallel data is converted into a bit-serial 622 Mbit/s or 155 Mbit/s data stream.

The on-chip PLL generates the 622 MHz or 155 MHz line rate clock from a subrate clock. For testing and applications which provide an external high-frequency bit clock, the internal clock generation PLL may be bypassed.

SX1405 Block Diagram Functional Description

Phase Locked Loop

The on-chip Phase Locked Loop (PLL) synthesizes the internal bit rate clock from the 19.44 / 38.66 / 77.78 MHz input reference clock. The PLL consists of a phase / frequency detector, loop filter, and Voltage Controlled Oscillator (VCO) nominally operating at 1.2 GHz. Dividers provide the internal clocks and a sub-rate clock output PLLCKP/PLLCKM (differential PECL) for phase comparison.

REFCK/REFCKM is the differential input PLL reference clock. The feedback, to close the loop of the PLL, is VARCK/VARCKM, the differential input variable clock. Both the REFCK and VARCK inputs can be driven by TTL levels if the "minus" input (REFCKM and VARCKM) are left open.

An Out Of Lock indicator (OOL) is driven HIGH if the PLL is not frequency locked with the input reference clock.

Parallel to Serial Conversion

In OC3 mode, converts a 4-bit (Nibble) 38.88 Mb/s or 8-bit (Byte) 19.44 Mb/s input to a differential 155.52 Mb/s serial data output. In OC12 mode, converts an 8-bit 77.76 Mb/s input to a differential 622.08 Mb/s serial data output. The input data is loaded into the Retime FF's by the Retiming Clock RETCK. Then the data is loaded into a shift register by PLLCK. The data shifted out is ordered MSB (DI1) first and LSB (DI8 or DI4) last.

Parity Check

The parity check provides a means of verifying the integrity of the parallel to serial converter with minimal overhead. The parity of the serial output data stream is compared to the value of the Even Parity Input (EPI). If a parity error is deteced, the Parity Error (PERR) output is set HIGH. The PERR pin has an Open Collector TTL Output and must be given a falling edge to reset the parity error detector.

SX1405 Control Signals

- Reset (RSTN) Used for testing and verification, the TTL outputs are set to Tri–State and all divider flip–flops and the parity generator are reset when RSTN = LOW. This also sets PERR HIGH and PERR must be given a falling edge to reset the parity error detector for normal operation. An internal pull–up is provided on RSTN allowing the device to operate normally if RSTN is not used.
- Low Speed Select (LSS) Selects data rate. LOW = OC-12 (622.08 Mb/s), HIGH = OC-3 (155.52 Mb/s). An

internal pull–up is provided on LSS allowing the device to operate in OC–3 mode if LSS is not used.

- Nibble / Byte Select (NBB) In OC–3 mode, selects between 4-bit (Nibble) and 8-bit (Byte) parallel data input format. LOW = Byte, HIGH = Nibble. An internal pull-up is provided on NBB allowing the device to operate in Nibble mode if NBB is not used.
- External Clock Select (ECSN) Allows external high–frequency bit clock to be applied and bypasses the internal clock generation circuit. LOW = External bit

clock. An internal pull–up is provided on ECSN allowing the device to operate normally if ECSN is not used.

- VCO Frequency Control Monitor (FCM) Single ended reference voltage output generated from the VCO control voltage. Typically 1.25V and varying from 0.25V to 2.25V.
- **Out of Lock Indicator (OOL)** Is set HIGH if the PLL is not frequency–locked to the input reference clock.

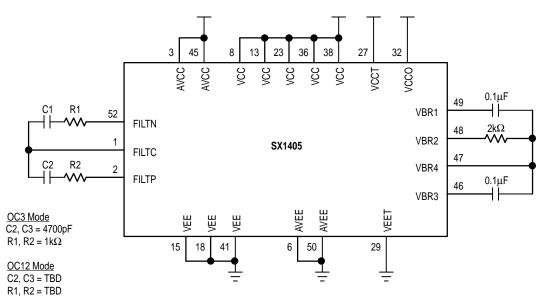


Figure 3. SX1405 Typical Operating Circuit

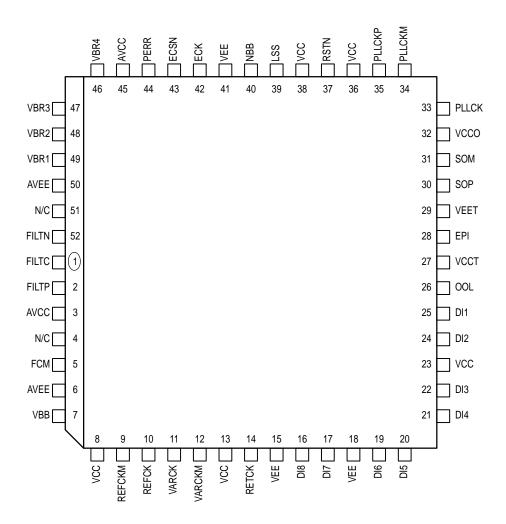


Figure 4. MC10SX1405 52-Lead Pinout (Top View)

TTL Compatible I/O RETCK 14 Re-Time Latch Clock DI8 16 Parallel Data Input DI7 17 Parallel Data Input DI6 19 Parallel Data Input DI6 19 Parallel Data Input DI6 19 Parallel Data Input DI4 21 Parallel Data Input DI4 21 Parallel Data Input DI4 22 Parallel Data Input DI2 24 Parallel Data Input DI1 25 Parallel Data Input DI2 24 Parallel Data Input DI4 25 Parallel Data Input DI4 25 Parallel Data Input DI4 26 Out of Lock Indicator Output OOL 26 Out of Lock Indicator Output STN 37 Reset Input LSS 39 Low Speed Select Input ECSN 43 External Clock Select Input PECL Compatible I/O VBB 7 VBE </th <th>Name</th> <th>Pin No</th> <th colspan="5">Description</th>	Name	Pin No	Description					
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ECK42External Clock InputAnalog I/OFCM5VCO Frequency Control MonitorVBR4-VBR146-49VCO Filter PinsFILTN52Loop Filter NegativeFILTC1Loop Filter CommonFILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output TTL 0V SupplyVCCO32Output PECL +5V Supply	PLLCKM	34	PLL Clock Out (19.44 / 38.88 / 77.76MHz) Minus					
Analog I/OFCM5VCO Frequency Control MonitorVBR4–VBR146–49VCO Filter PinsFILTN52Loop Filter NegativeFILTC1Loop Filter CommonFILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output PECL +5V SupplyVCCO32Output PECL +5V Supply	PLLCKP	35	PLL Clock Out (19.44 / 38.88 / 77.76MHz) Plus					
FCM5VCO Frequency Control MonitorVBR4–VBR146–49VCO Filter PinsFILTN52Loop Filter NegativeFILTC1Loop Filter CommonFILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVEE27Output TTL +5V SupplyVEET29Output PECL +5V SupplyVCCO32Output PECL +5V Supply	ECK	42	External Clock Input					
VBR4-VBR146-49VCO FIlter PinsFILTN52Loop Filter NegativeFILTC1Loop Filter CommonFILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output PECL +5V SupplyVCCO32Output PECL +5V Supply	Analog I/O	-						
FILTN52Loop Filter NegativeFILTC1Loop Filter CommonFILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output TTL 0V SupplyVCCO32Output PECL +5V Supply	FCM	5	VCO Frequency Control Monitor					
FILTC1Loop Filter CommonFILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output TTL 0V SupplyVCCO32Output PECL +5V Supply	VBR4–VBR1	46–49	VCO FIlter Pins					
FILTP2Loop Filter PositivePower and Ground PinsAVCC3, 45Analog +5V SupplyAVEE6, 50Analog 0V SupplyVCC8, 13, 23, 36, 38PECL +5V SupplyVEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output TTL 0V SupplyVCCO32Output PECL +5V Supply	FILTN	52	Loop Filter Negative					
Power and Ground Pins AVCC 3, 45 Analog +5V Supply AVEE 6, 50 Analog 0V Supply VCC 8, 13, 23, 36, 38 PECL +5V Supply VEE 15, 18, 41 PECL 0V Supply VCCT 27 Output TTL +5V Supply VEET 29 Output TTL 0V Supply VCCO 32 Output PECL +5V Supply	FILTC	1	Loop Filter Common					
AVCC 3, 45 Analog +5V Supply AVEE 6, 50 Analog 0V Supply VCC 8, 13, 23, 36, 38 PECL +5V Supply VEE 15, 18, 41 PECL 0V Supply VCCT 27 Output TTL +5V Supply VEET 29 Output TTL 0V Supply VCCO 32 Output PECL +5V Supply	FILTP	2	Loop Filter Positive					
AVEE 6, 50 Analog 0V Supply VCC 8, 13, 23, 36, 38 PECL +5V Supply VEE 15, 18, 41 PECL 0V Supply VCCT 27 Output TTL +5V Supply VEET 29 Output TTL 0V Supply VCCO 32 Output PECL +5V Supply	Power and Groun	nd Pins						
VCC 8, 13, 23, 36, 38 PECL +5V Supply VEE 15, 18, 41 PECL 0V Supply VCCT 27 Output TTL +5V Supply VEET 29 Output TTL 0V Supply VCCO 32 Output PECL +5V Supply	AVCC	3, 45	Analog +5V Supply					
VEE15, 18, 41PECL 0V SupplyVCCT27Output TTL +5V SupplyVEET29Output TTL 0V SupplyVCCO32Output PECL +5V Supply	AVEE	6, 50	Analog 0V Supply					
VCCT27Output TTL +5V SupplyVEET29Output TTL 0V SupplyVCCO32Output PECL +5V Supply	VCC	8, 13, 23, 36, 38	PECL +5V Supply					
VEET 29 Output TTL 0V Supply VCCO 32 Output PECL +5V Supply	VEE	15, 18, 41	PECL 0V Supply					
VCCO 32 Output PECL +5V Supply	VCCT	27	Output TTL +5V Supply					
	VEET	29	Output TTL 0V Supply					
Pasanyad	VCCO	32	Output PECL +5V Supply					
	Reserved							
N/C 4, 51 No Connection	N/C	4, 51	No Connection					

Table 1. SX1405 Pin Descriptions

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
VCC, VCCO, VCCT, AVCC	Power Supply (VEE, VEET, AVEE, GVEE = 0V)		-0.5 to +6.5	V
VIN	Input Voltage (VEE, VEET, AVEE, GVEE = 0V)		-0.5 to +6.5	V
IOUT	PECL Output Current	Continuous Surge	50 100	mA
IOUT-TTL	TTL Output Current		5	mA
TSTG	Storage Temperature		-50 to +175	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
VCC, VCCO, VCCT, AVCC	Power Supply (VEE, VEET, AVEE, GVEE = 0V)	5V ±5%	V
ICC	Device Current Drain	100	mA
ТА	Operating Temperature	-40 to +85	°C
TJ	Junction Temperature	125	°C

TTL DC CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V ±5%)

Symbol	Characteristic	Min	Тур	Max	Unit	Condition
IIH	Input HIGH Current			20	μΑ	$VIN = V_{CC}$
IIL	Input LOW Current			-0.6	mA	VIN = 0.5V
VOH	Output HIGH Voltage REP, ROD EDO, OOL	2.5 2.5			V	IOH = -2mA IOH = -300μA
VOL	Output LOW Voltage			0.5	V	IOL = 5mA
VIH	Input HIGH Voltage	2.0			V	
VIL	Input LOW Voltage			0.8	V	
IOZ	Tri–State Current			±50	μΑ	

100E PECL DC CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = $5.0V \pm 5\%$)

Symbol	Characteristic	Min	Тур	Max	Unit	Condition
IIH	Input HIGH Current			200	mA	
IIL	Input LOW Current	0.5			mA	
VOH	Output HIGH Voltage	3.98		4.19	V	NOTE 1.
VOL	Output LOW Voltage	3.19		3.45	V	NOTE 1.
VIH	Input HIGH Voltage	3.93		4.19	V	NOTE 1.
VIL	Input LOW Voltage	3.19		3.43	V	NOTE 1.

1. PECL levels are referenced to VCC and will vary 1:1 with the Power Supply. The Outputs are loaded with an equivalent 50Ω termination to +3.0V. The values shown are for VCC = VCCT = VCCO = AVCC = 5.0V.

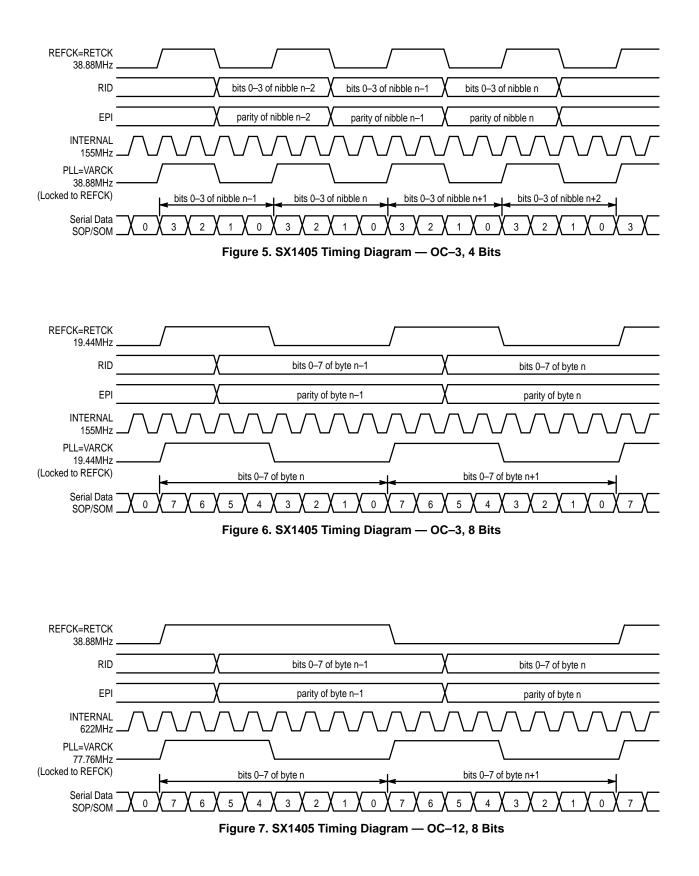
Symbol	Characteristic	Min	Тур	Max	Unit	Condition
IFILT	Loop Filter Currents (FILTP-FILTN)	300 500		500 300	μΑ	PD Up PD Down
Kdt	Combined Phase Detector TZA Gain	45		80	μA/rad	
ADV	Loop Filter Amplifier Large Signal Differential Voltage Amplification	100	250		V/V	
φE	Phase Error	-0.45		0.45	radians	
VFCM	FCM Amplitude Range	0.3		2.2	V	
	FCM Locked PLL Range	0.65		1.85	V	
	FCM Shorted	1.1		1.4	V	FILTP, FILTN Shorted
EFCM	FCM Error	-100		100	mV	
KFCM	FCM Gain	0.45		0.55	gain	
RO	FCM Output Impedance		5000		Ω	
fVCO	VCO Frequency	700	1244	1800	MHz	2000Ω (1%) – EXT. R
	VCO Frequency Shorted	1000		1450	MHz	FILTP, FILTN Shorted
КО	VCO Gain	120	220	260	MHz/V	2000Ω (1%) – EXT. R
KOVCC	VCC Supply (AVCC) Sensitivity	-80		80	MHz/V	0 < fVCC < 10MHz
φVCO	VCO Phase Noise		-30		dBc/Hz	at f = 1kHz
			-90		dBc/Hz	at f = 1kHz

PLL COMPONENT CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = $5.0V \pm 5\%$)

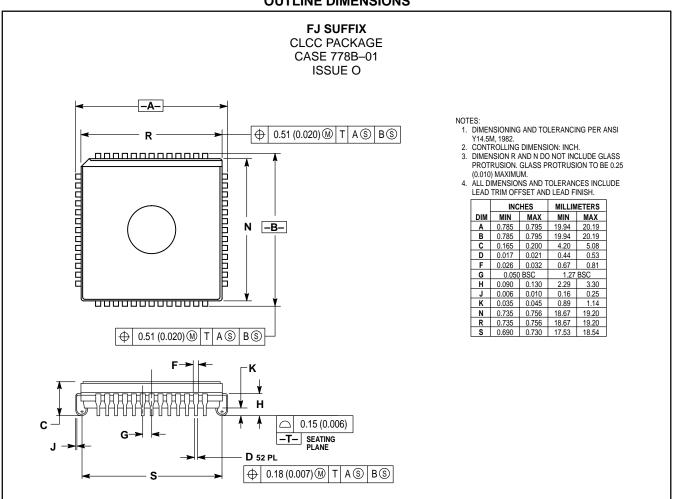
AC CHARACTERISTICS (VCC = VCCT = VCCO = AVCC = 5.0V +5%)

Symbol	Characteristic	Min	Тур	Max	Unit	Condition
tr, tf	PECL Rise/Fall Time			1.6	nS	20–80%, 50 Ω to VCC–2V
tr, tf	TTL Rise/Fall Time			5.0	nS	20–80%, 50 Ω to VCC–2V

MC10SX1405



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